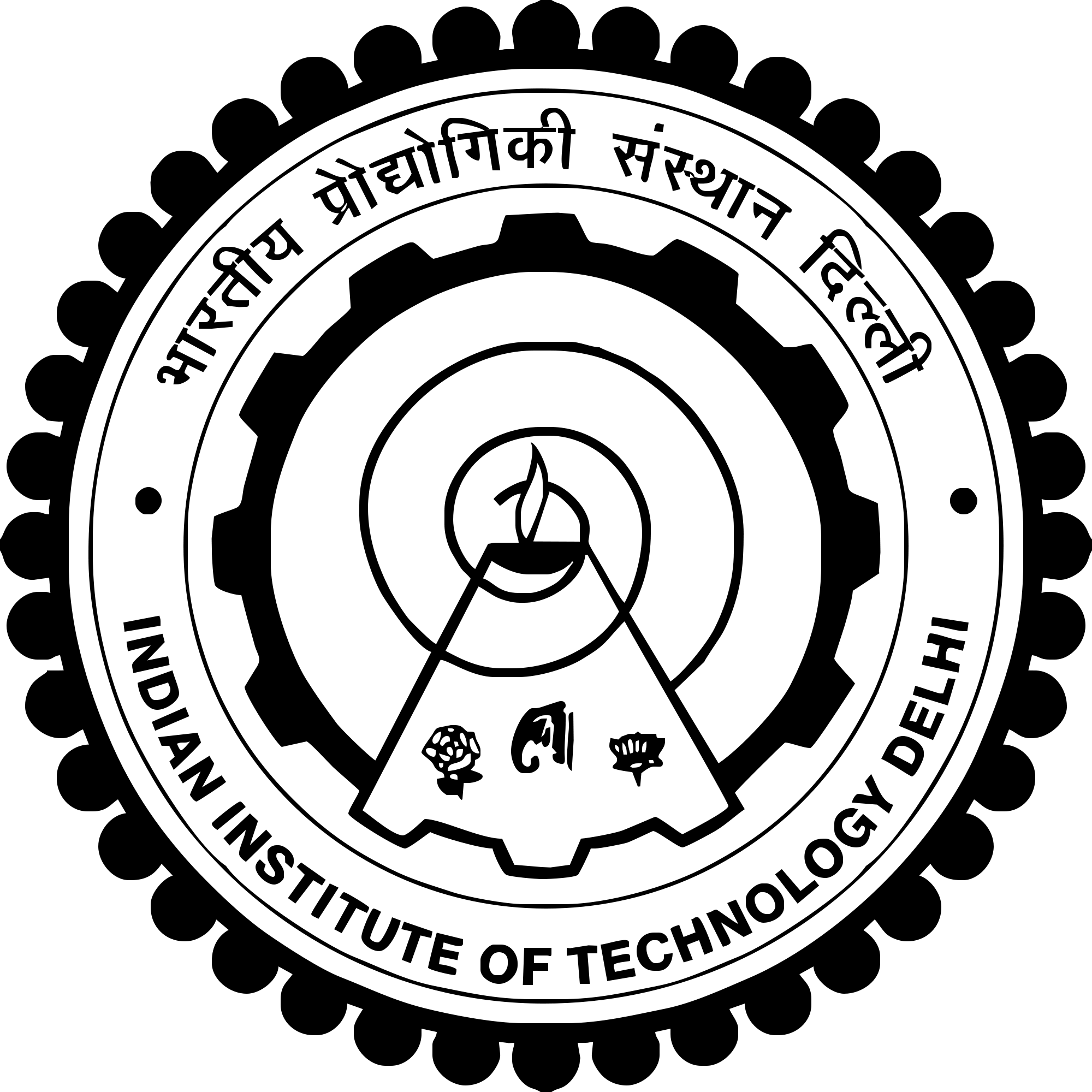
**Experiment-1 ELL304: Device Characterisation**

Submission Date: 23rd Aug 2024

Performed by:

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**Aim of the experiment:**

* Measure and analyze the drain current (ID) vs. gate-source voltage (VGS) for MN1 to estimate the threshold voltage (VT).
* Measure and plot ID vs. drain-source voltage (VDS) for MN1 under different VGS values to understand its operating regions.
* Assess CMOS inverter performance by analyzing output waveform changes with varying input frequencies, particularly the transition from a square to a sine wave.

**Equipment Required:**

* CD4007 IC
* Breadboard
* Signal Generator
* DC Voltage Source
* Wire Stripper
* Connecting Wires
* Oscilloscope
* Probes and Cables
* Resistors

**Theory:**

The drain current (ID) through a MOSFET (nMOS) is given as:

0, VGS < VT: Cut-off Region

µn Cox ((VGS – VT)VDS – V2DS/2), VGS < VT and VDS < (VGS – VT): Triode Region

µn Cox (VGS – VT)2, VGS > VT and VDS > (VGS – VT): Saturation Region

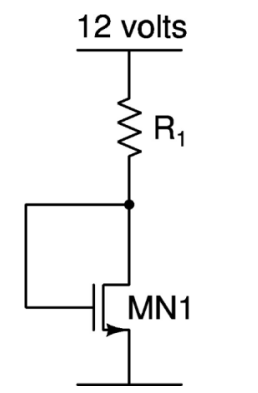
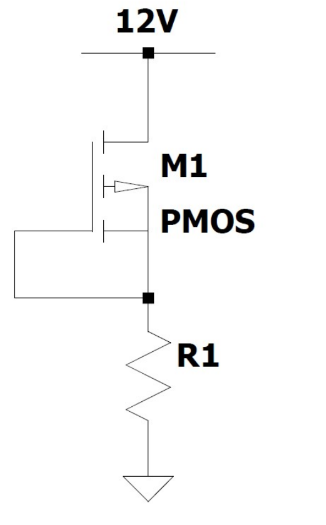
In this experiment, we focus on characterizing MOSFET devices using the CD4007 integrated circuit, which includes n-channel and p-channel MOS transistors. The behavior of these transistors is analyzed by studying the relationship between the drain current (ID) and both the gate-source voltage (VGS) and drain-source voltage (VDS).

For an n-channel MOSFET (MN1), the drain current increases with VGS until it reaches the threshold voltage (VT), after which the MOSFET enters the saturation region where ID becomes relatively independent of VDS. This characteristic helps determine the operational regions of the MOSFET: cutoff, linear, and saturation.

The experiment also involves analyzing a CMOS inverter, which is constructed using complementary MOS transistors (n-MOS and p-MOS). The CMOS inverter switches states based on the input voltage, producing a square wave output under normal operation. However, at higher input frequencies, the output waveform may degrade into a sine wave due to the limited switching speed of the transistors, which indicates the frequency limitations of the inverter circuit.

**Part-1:**

**Procedure:**

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* Circuit was connected as shown in circuit diagram. Pin 7 (source) was connected to ground and pins 6 (gate) and 8 (drain) were shorted. Pin 8 was then connected to resistor R1, whose other end was connected to source VDD
* Oscilloscope probes were connected to pin 8 and ground respectively and voltage was measured.
* Readings were taken for different values of R1.
* Similar steps are repeated for pMOS.

**Observations:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **V\_GS (NMOS) in V** | **I\_D (NMOS)**  **in A** | **V\_GS (PMOS)**  **in V** | **I\_D (PMOS)**  **in A** | R1 (in kΩ) |
| 2.88 | 0.914914 | 2.87 | 0.792812 | 8.18 |
| 4.25 | 3.604651 | 4.38 | 3.544186 | 2.15 |
| 1.86 | 0.183032 | 2.22 | 0.181949 | 55.4 |
| 1.67 | 0.102277 | 1.88 | 0.098911 | 101 |
| 2.67 | 0.603195 | 2.48 | 0.351917 | 10.33 |
| 1.84 | 0.176542 | 1.82 | 0.176542 | 57.55 |
| 1.2 | 0.066924 | 1.5 | 0.067568 | 155.4 |
| 1.64 | 0.094889 | 1.34 | 0.097637 | 109.18 |

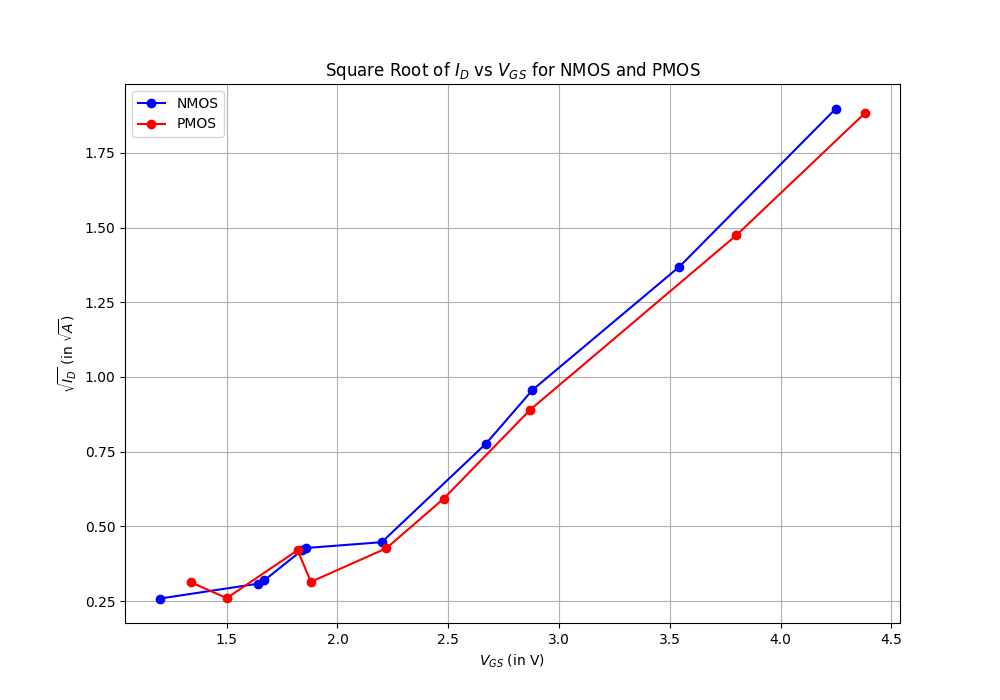
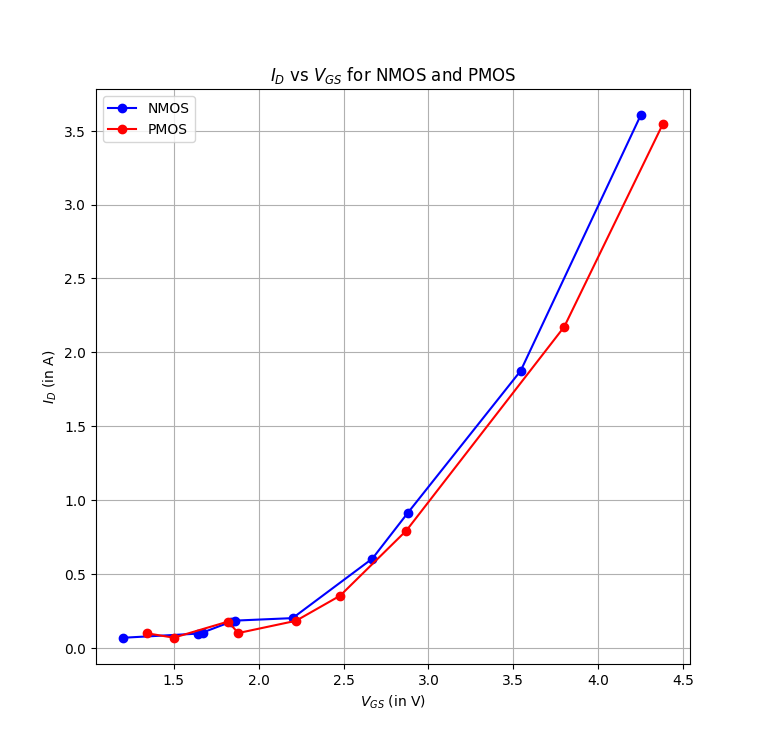
**A white board with wires on it

Description automatically generatedBreadboard Setup:**

**A white board with wires and a pair of clamps

Description automatically generated**

**Graphs:**

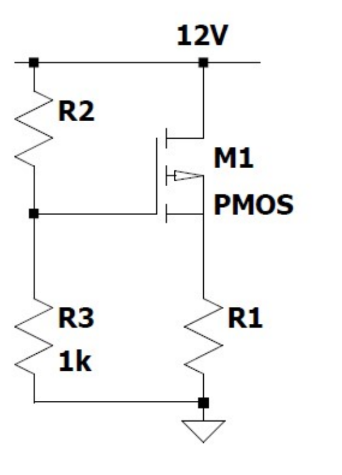
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IG vs VGS IG vs VGS

**Conclusions:**

* From the IG vs VGS graph, we obtain VT of NMOS as 1.12V and PMOS as 0.94V.
* We observe that, in the saturation region, ID increases with VGS in NMOS and VSG in PMOS and the relation is almost quadratic as expected theoretically.

**Part-2:**

**Procedure:**

**A diagram of a circuit

Description automatically generated**

* Circuit was connected as shown in circuit diagram. Pin 7 (source) was connected to ground. Pin 8 (drain) was connected to resistor R1. Pin 6 (gate) was connected to two resistors R2 and 1kΩ. The other ends of resistors were connected as shown.
* Oscilloscope probes were connected at pin 8 and ground respectively and voltage readings were taken.
* Readings were taken for different values of R2, varying R1 for each.
* Similar steps are repeated for pMOS.

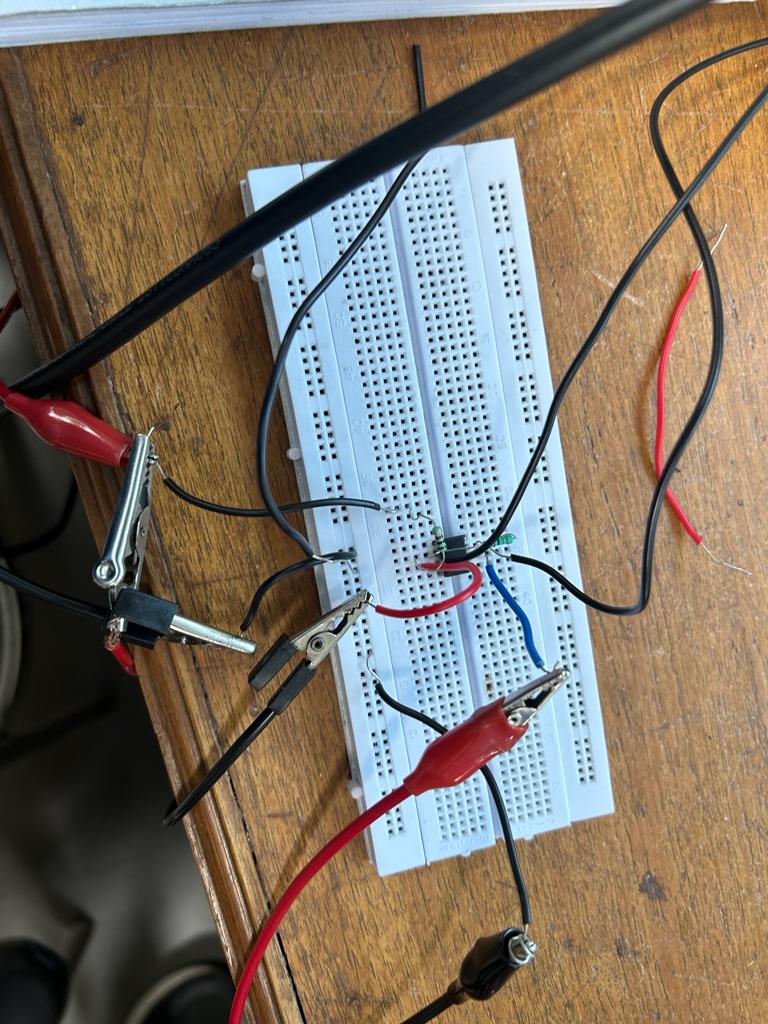
**Observations:**

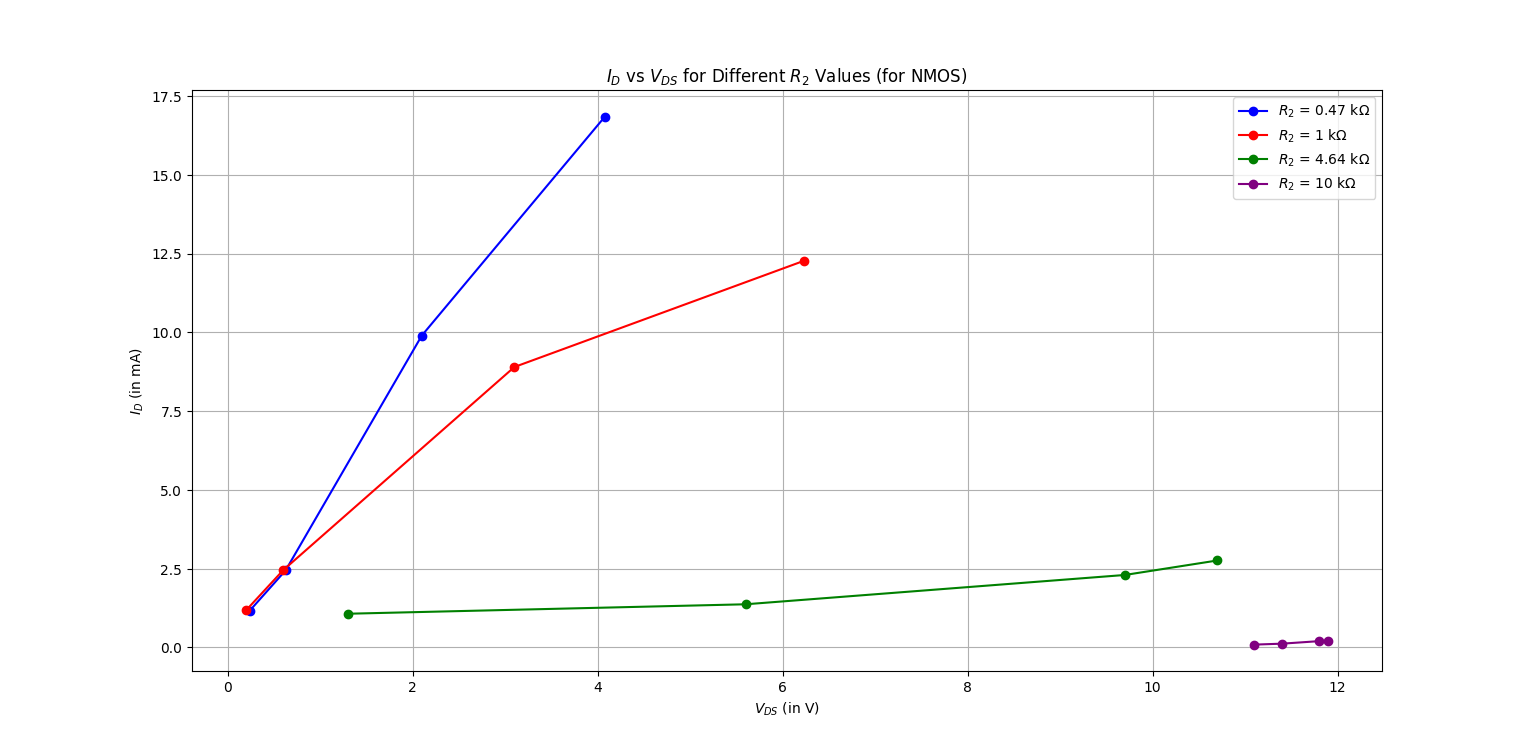
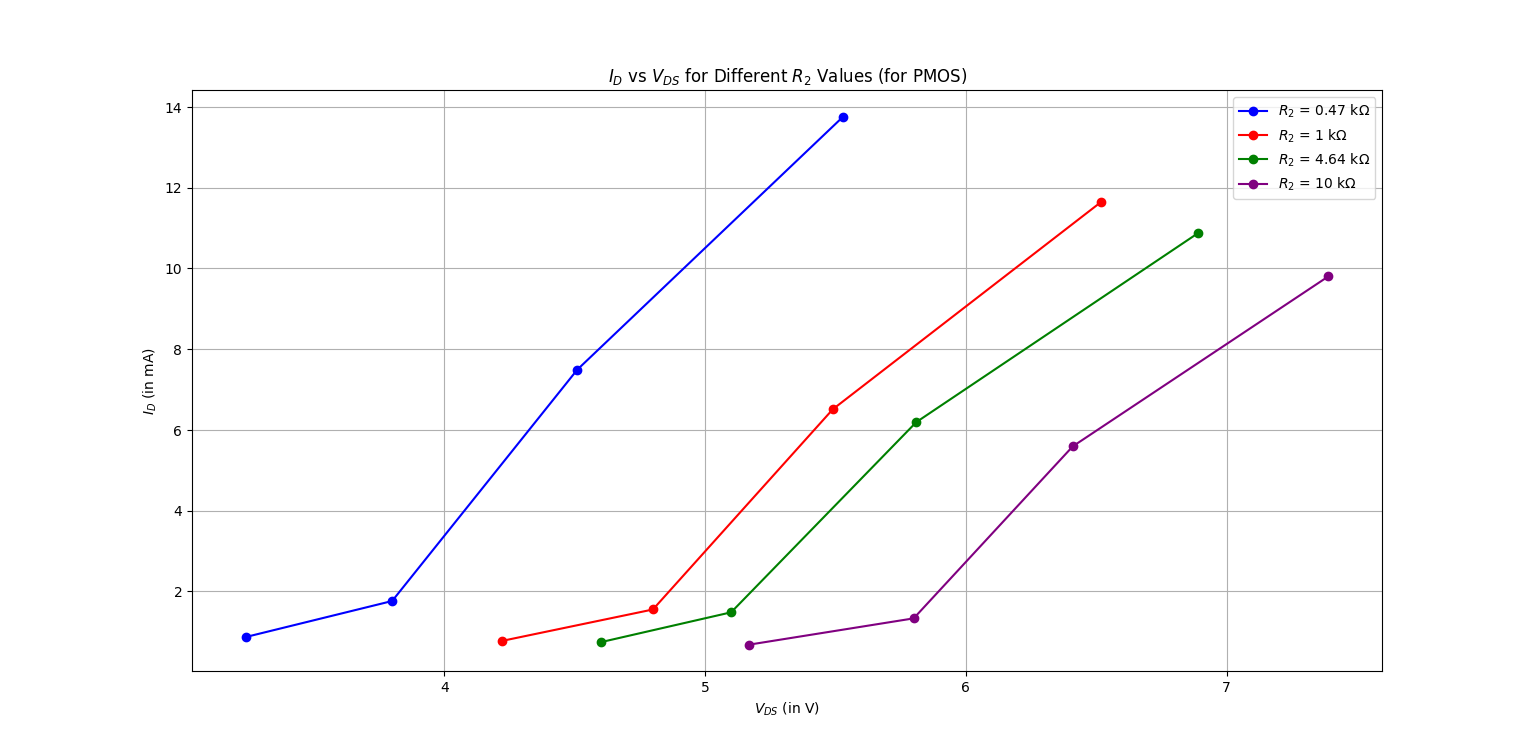
For nMOS,

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **R1 (in kΩ)** | **R2 (in kΩ)** | **V\_DS (in V)** | **I\_D (in mA)** | **V\_GS (in V)** |
| 0.47 | 0.47 | 4.08 | 16.85 | 8.16 |
| 1 | 0.47 | 2.1 | 9.9 | 8.16 |
| 4.64 | 0.47 | 0.628 | 2.45 | 8.16 |
| 10 | 0.47 | 0.24 | 1.17 | 8.16 |
| 0.47 | 1 | 6.23 | 12.27 | 6 |
| 1 | 1 | 3.1 | 8.9 | 6 |
| 4.64 | 1 | 0.6 | 2.45 | 6 |
| 10 | 1 | 0.2 | 1.18 | 6 |
| 0.47 | 4.64 | 10.7 | 2.76 | 2.1 |
| 1 | 4.64 | 9.7 | 2.3 | 2.1 |
| 4.64 | 4.64 | 5.6 | 1.37 | 2.1 |
| 10 | 4.64 | 1.3 | 1.07 | 2.1 |
| 0.47 | 10 | 11.9 | 0.21 | 1.09 |
| 1 | 10 | 11.8 | 0.2 | 1.09 |
| 4.64 | 10 | 11.4 | 0.12 | 1.09 |
| 10 | 10 | 11.1 | 0.09 | 1.09 |

For pMOS,

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **R1 (kΩ)** | **R2 (kΩ)** | **V\_DS** | **I\_D (mA)** | **V\_GS (in V)** |
| 0.47 | 0.47 | 5.53 | 13.76 | 8.16 |
| 1 | 0.47 | 4.51 | 7.49 | 8.16 |
| 4.64 | 0.47 | 3.8 | 1.76 | 8.16 |
| 10 | 0.47 | 3.24 | 0.87 | 8.16 |
| 0.47 | 1 | 6.52 | 11.65 | 6 |
| 1 | 1 | 5.49 | 6.51 | 6 |
| 4.64 | 1 | 4.8 | 1.55 | 6 |
| 10 | 1 | 4.22 | 0.77 | 6 |
| 0.47 | 4.64 | 6.89 | 10.87 | 2.1 |
| 1 | 4.64 | 5.81 | 6.19 | 2.1 |
| 4.64 | 4.64 | 5.1 | 1.48 | 2.1 |
| 10 | 4.64 | 4.6 | 0.74 | 2.1 |
| 0.47 | 10 | 7.39 | 9.8 | 1.09 |
| 1 | 10 | 6.41 | 5.59 | 1.09 |
| 4.64 | 10 | 5.8 | 1.33 | 1.09 |
| 10 | 10 | 5.17 | 0.68 | 1.09 |

**Breadboard Setup:**

**Graph:**

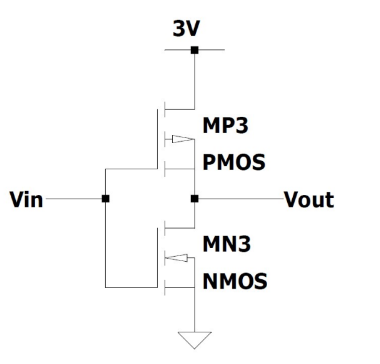
nMOS pMOS

**Conclusions:**

* We found that as VGS increases, the value of ID also increases.
* We also observe that as VGS increases, ID vs VDS does not become constant after saturation point as we have taken combination of very few resistors, and we do not cross the saturation point.

**Part-3:**

**Procedure:**

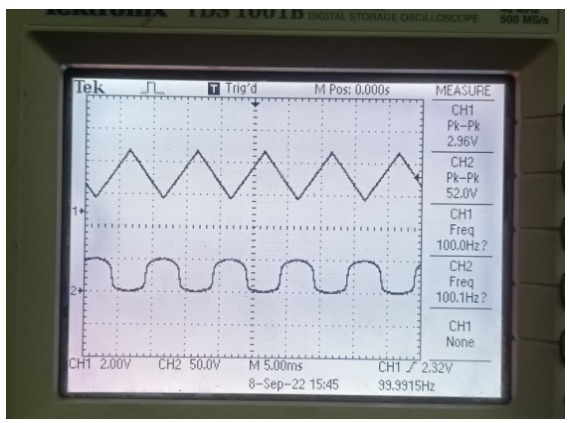
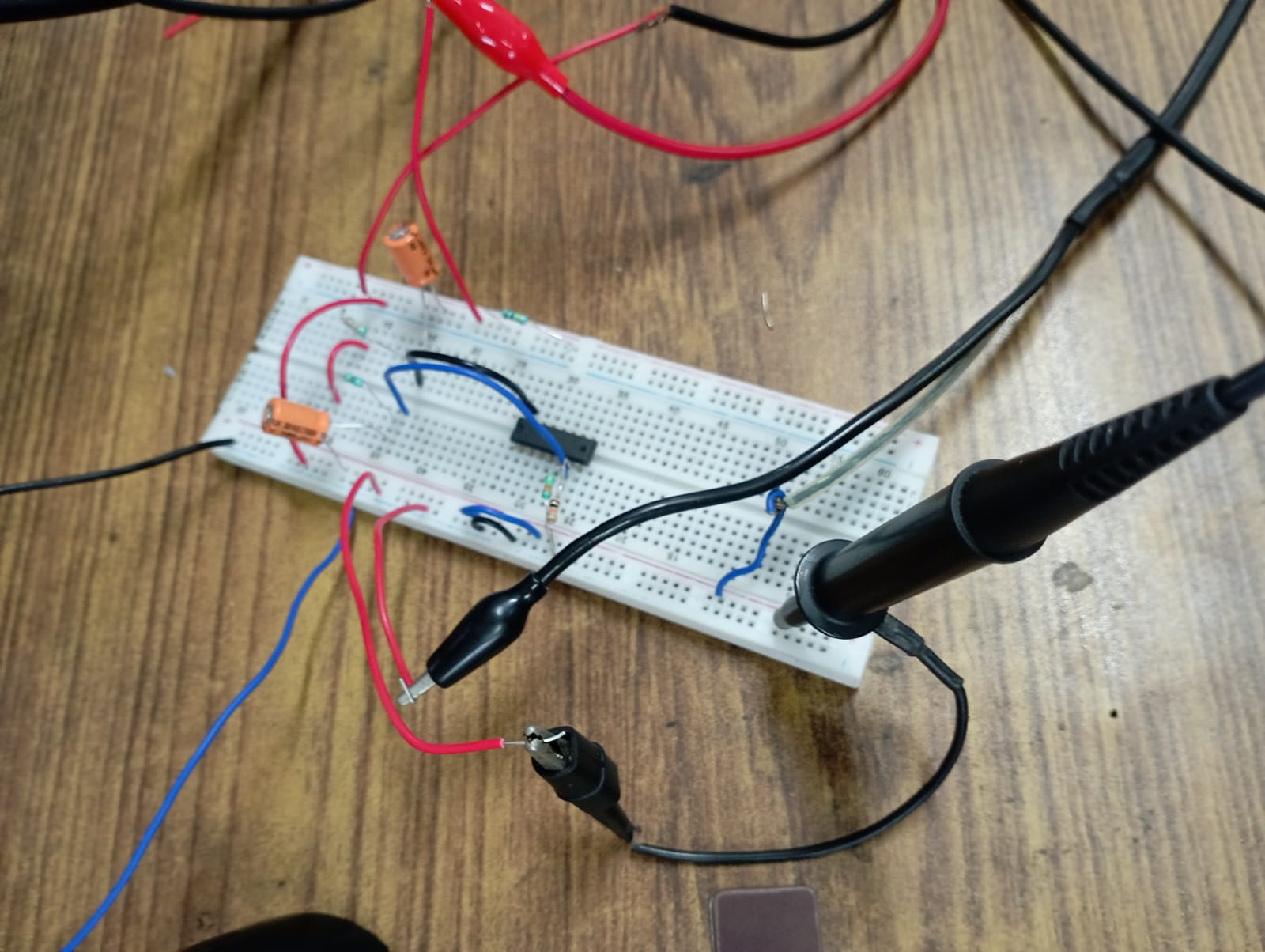


* MP1 and MP3 are configured as CMOS inverter. The pins were correctly connected as per circuit diagram shown.
* Different DC voltages were applied at gate and the drain voltages were noted.
* Now, a triangular wave from function generator was applied at gate and frequency was increased till the output at drain was no longer a square wave.

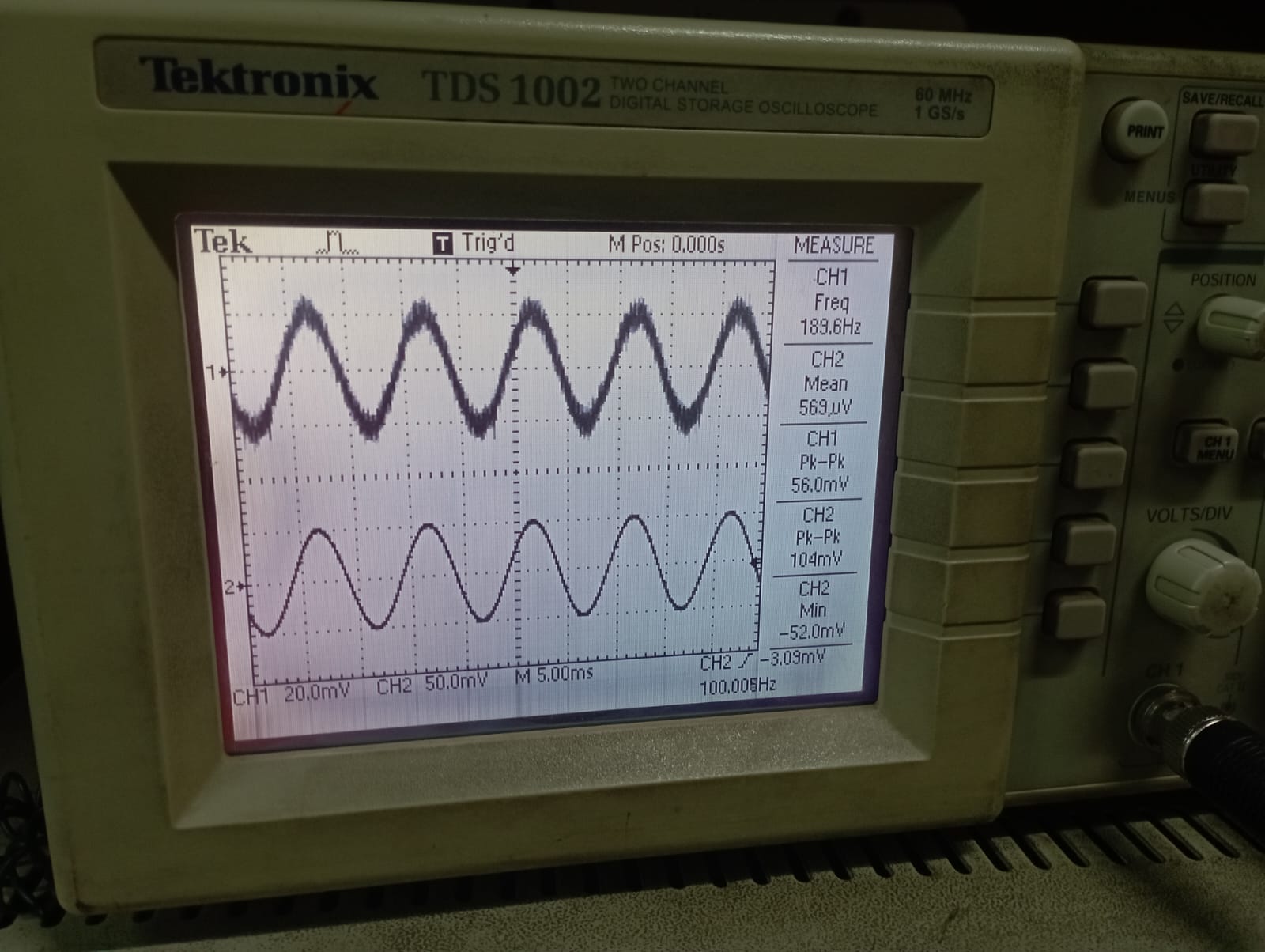
**Observations:**

|  |  |
| --- | --- |
| **Vin (in mV)** | **Vout (in mV)** |
| 2 | 4.2 |
| 3 | 3.6 |
| 4 | 3.41 |
| 5 | 3.4 |
| 6 | 1.69 |
| 7 | 1.12 |
| 8 | 0.808 |
| 9 | 0.531 |
| 10 | 0.205 |
| 11 | 0.009 |
| 12 | 0.0083 |

**Breadboard Setup and Oscilloscope:**

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**A close-up of a device

Description automatically generated**

**Conclusions:**

* As the frequency increases, the transistors can't switch on and off fast enough due to small delays in the circuit. This causes the output to be less strong or "amplified," leading to a decrease in gain.
* When the frequency is too high, the circuit can't keep up with the fast changes, so the sharp edges of the square wave start to round off, making the output look more like a sine wave (around a frequency of 1MHz).